

IN THE CLAIMS:

1. (currently amended) A method of operating a graphics system having a sequence of at least two discrete performance levels with each performance level being defined by a core clock rate of a graphics processing unit and a memory clock rate, the method comprising:

monitoring a percentage of clock cycles at one or more points within a graphics processor core clock domain for which one or more stages of a graphics pipeline are stalled waiting for data inputs from upstream stages of the graphics pipeline as an indicator of utilization and determining whether the graphic pipeline is under-utilized or over-utilized based on comparing the percentage of clock cycles for which there is a stall within one or more blocks of the graphics pipeline against a first threshold level of stalls and a second threshold level of stalls with the first threshold level of stalls being greater than the second threshold level of stalls;

increasing the performance level in response to detecting an over-utilization condition corresponding to the percentage of stalled clock cycles exceeding the first threshold level in order to increase the clock rate in the graphics processor core clock domain and decreasing the performance level in response to detecting an under-utilization condition corresponding to the percentage of stalled clock cycles being no greater than the second threshold level to decrease the clock rate in the graphics processor core clock domain; and

operating the graphics system at the core clock rate and memory clock rate associated with the selected performance level, the selected performance level being a minimum performance level sufficient to maintain the display rate within a normal range, the graphics pipeline being in the graphics processor core clock domain such that the performance level affects the clock rate of the graphics pipeline.

2-20. (cancelled)

21. (currently amended) A method of operating a graphics system having a sequence of at least two discrete performance levels where each performance level is defined by a core clock rate of a graphics processing unit and a memory clock rate, the performance levels including a high performance level for processing complex three-dimensional graphical images and at least

one lower power, lower performance level for processing less complex graphical images, the method comprising:

monitoring as a function of time a percentage of clock cycles at one or more points within a graphics processor core clock domain for which one or more stage of a graphics pipeline are stalled waiting for data inputs from upstream stages of the graphics pipeline as an indicator of utilization and determining whether the graphic pipeline is under-utilized or over-utilized based on comparing the percentage of clock cycles for which there is a stall in the graphics pipeline against a first threshold level of stalls and a second threshold level of stalls with the first threshold level of stalls being greater than the second threshold level of stalls;

in response to detecting a level of utilization greater than an over-utilization threshold for which a display rate of the graphics system is likely to be significantly decreased below a normal display rate, selecting a higher performance level to increase a clock rate in the graphics processor core clock domain, the over-utilization threshold corresponding to the percentage of stalled clock cycles exceeding the first threshold level;

in response to detecting a level of utilization below an under-utilization threshold, selecting a lower performance level to reduce the clock rate in the graphics processor core clock domain to reduce power required by the graphics system, the under-utilization threshold corresponding to the percentage of stalled clock cycles being no greater than the second threshold level; and

operating the graphics system at the core clock rate and memory clock rate associated with the selected performance level, the selected performance level being a minimum performance level sufficient to maintain the display rate within the normal range, the graphics pipeline being in the graphics processor core clock domain such that the performance level affects the clock rate of the graphics pipeline.

22-24. (cancelled)

25. (currently amended) A graphics system, comprising:

a graphics processor having a sequence of at least two discrete performance levels where each performance level is defined by a graphics processor core clock rate of a graphics processing unit and a memory clock rate;

a graphics memory coupled to said graphics processor by a graphics bus and operable at said memory clock rate;

a performance level controller, said performance level controller configured to monitor, as function of time a percentage of clock cycles at one or more points within a graphics processor core clock domain for which one or more stages of a graphics pipeline are stalled waiting for data inputs from upstream stages of the graphics pipeline as an indicator of utilization and determining whether the graphic pipeline is under-utilized or over-utilized by comparing the percentage of clock cycles for which there is a stall in the graphics pipeline against a first threshold level of stalls and a second threshold levels of stalls with the first threshold level of stalls being greater than the second threshold level of stalls; and

said performance level controller configured to increase said performance level to increase a clock rate in the graphics processor core clock domain to avoid over-utilization of said graphics pipeline, in response to detecting the percentage of stalled clock cycles exceeding the first threshold level;

said performance level controller configured to decrease said performance level from a high performance level to a lower performance level to decrease the clock rate in the graphics processor core clock domain to avoid under-utilization of said graphics pipeline in response to detecting the first threshold percentage of stalled clock cycles being no greater than the second threshold level;

the graphics system operating at the core clock rate and memory clock rate associated with the performance level selected by the performance level controller, the selected performance level being a minimum performance level capable of maintaining the display rate within a normal range, the graphics pipeline being in the graphics processor core clock domain such that the performance level affects the clock rate of the graphics pipeline.

26-27. (cancelled)

28. (previously presented) The method of claim 1, wherein said at least two discrete performance levels include a low power two-dimensional graphics performance level, a standard two-dimensional graphics performance level, a low power three-dimensional graphics performance level, and a high performance three-dimensional graphics performance level.

29. (previously presented) The method of claim 21, wherein said at least two discrete performance levels include a low power two-dimensional graphics performance level, a standard two-dimensional graphics performance level, a low power three-dimensional graphics performance level, and a high performance three-dimensional graphics performance level.

30. (previously presented) The graphics system of claim 25, wherein the performance levels include a low power two-dimensional graphics performance level, a standard two-dimensional graphics performance level, a low power three-dimensional graphics performance level, and a high performance three-dimensional graphics performance level.